

CLAIMS:

1. A static tie switch operable to selectively allow power flow between a first bus and a second bus, the switch comprising:

5 a first feeder operable to be connected to the first bus;

a second feeder operable to be connected to the second bus; and

10 a solid-state interconnection between the feeders and operable to selectively tie the first bus to the second bus and selectively isolate the first bus from the second bus without the use of moving parts between the buses, thereby reliably allowing power to flow between the buses.

2. The switch as set forth in claim 1, wherein the interconnection includes a pair of silicon controlled rectifiers each operable to handle all of the power flow between the buses.

15 3. The switch as set forth in claim 1, wherein the feeders and the interconnection include three phases.

20 4. The switch as set forth in claim 3, wherein the interconnection includes three pairs of silicon controlled rectifiers (SCR)s each operable to handle all of the power flow between the buses for one of the phases.

25 5. The switch as set forth in claim 4, wherein each pair of SCRs electrically couples a different one of the phases of the first bus with a corresponding phase of the second bus.

30 6. The switch as set forth in claim 1, wherein the feeders and the interconnection are rated for a voltage selected from the group consisting of 120, 240, 208 and 480 Volts.

30 7. The switch as set forth in claim 1, wherein the feeders and the interconnection are rated for a voltage selected from the group consisting of 2.3, 4.16, 12.47, 13.8, 25, or 34.5 Kilo Volts.

8. The switch as set forth in claim 1, further including a controller to bias the interconnection, thereby shorting between the buses.

9. The switch as set forth in claim 8, wherein the controller is further
5 operable to control a breaker in order to isolate a power source.

10. A static tie switch operable to be connected between a first source, a second source, a first load, and a second load, the switch comprising:

5 a first output operable to be connected to the first load;

 a second output operable to be connected to the second load;

 a first input operable to be connected to the first source, such that during normal operations the first input is connected to the first output with the first source supplying power to the first load;

10 a second input operable to be connected to the second source, such that during normal operations the second input is connected to the second output with the second source supplying power to the second load;

 a solid-state interconnection between the inputs and outputs including three pairs of silicon controlled rectifiers (SCR)s operable to selectively tie the first output to the second input and selectively tie the second output to the first input;

15 a first circuit breaker operable to be connected between the first input and the interconnection;

 a second circuit breaker operable to be connected between the second input and the interconnection;

20 a controller operable to control the interconnection and the breakers to isolate either one of the inputs, wherein the controller is able to manipulate the SCRs in order to tie both of the outputs to a selected one of the inputs;

 a first bypass operable to selectively connect the first input directly to the first output, thereby bypassing the interconnection and the first circuit breaker; and

25 a second bypass operable to selectively connect the second input directly to the second output, thereby bypassing the interconnection and the second circuit breaker.

30 11. The switch as set forth in claim 10, wherein the feeders and the interconnection are rated for a voltage selected from the group consisting of 120, 240, 208 and 480 Volts.

12. The switch as set forth in claim 10, wherein the feeders and the interconnection are rated for a voltage selected from the group consisting of 2.3, 4.16, 12.47, 13.8, 25, or 34.5 Kilo Volts.

5 13. The switch as set forth in claim 10, wherein each pair of SCRs electrically couples a phase of the first bus with a phase of the second bus.